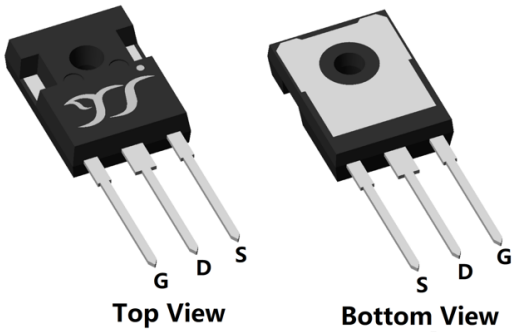
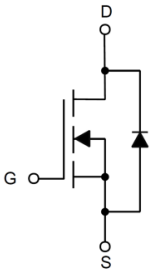
N-Channel Enhancement Mode Field Effect Transistor



TO-247



Product Summary

- V_{DS} 60V
- I_D 120A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜9.8mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜13.5mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Motor Drive Application
- DC-DC convertor

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	60	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	I_D	14	A
		T_A=100℃		8.8	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃		120	
		T_C =100℃		75	
Pulsed Drain Current	T_C=25℃, t_p=100μs		I_{DM}	500	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=70A		EAS	1225	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	3.1	W
		T_A=100℃		1.2	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		277	
		T_C =100℃		111	
Junction and Storage Temperature Range			T_J , T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	35	40	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.36	0.45	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJN9D8N06AQ	B1	YJN9D8N06A	30	360	1800	Tube

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60	-	-	V
		V_{GS}= 0V, I_D=1mA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
		V_{DS}=60V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.1	1.6	2.1	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	-	7.4	9.8	mΩ
		V_{GS}=4.5V, I_D=25A	-	10	13.5	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	2	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	120	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V, f=1MHz	-	4930	-	pF
Output Capacitance	C_{oss}		-	1460	-	
Reverse Transfer Capacitance	C_{rss}		-	155	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=30V, I_D=50A	-	125	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	
Gate-Drain Charge	Q_{gd}		-	36	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A, di/dt=100A/us	-	132	-	nC
Reverse Recovery Time	t_{rr}		-	67	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=30V, I_D=50A R_{GEN}=2.7Ω	-	18	-	ns
Turn-on Rise Time	t_r		-	100	-	
Turn-off Delay Time	$t_{D(off)}$		-	88	-	
Turn-off fall Time	t_f		-	44	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured in the still air environment with TA =25℃.The maximum allowed junction temperature of 150℃.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

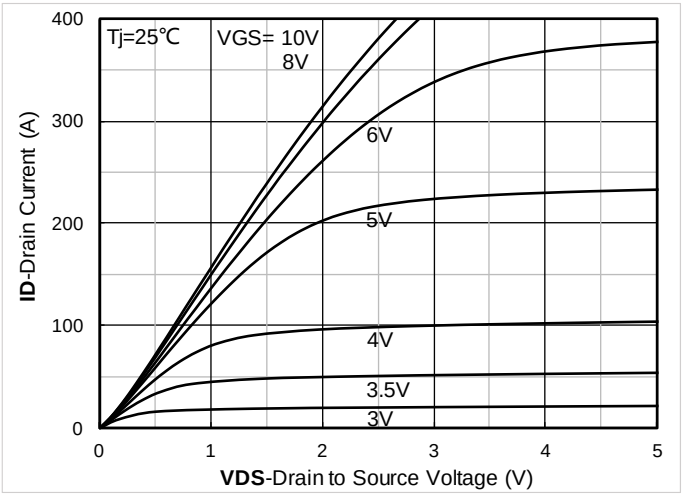


Figure 1. Output Characteristics

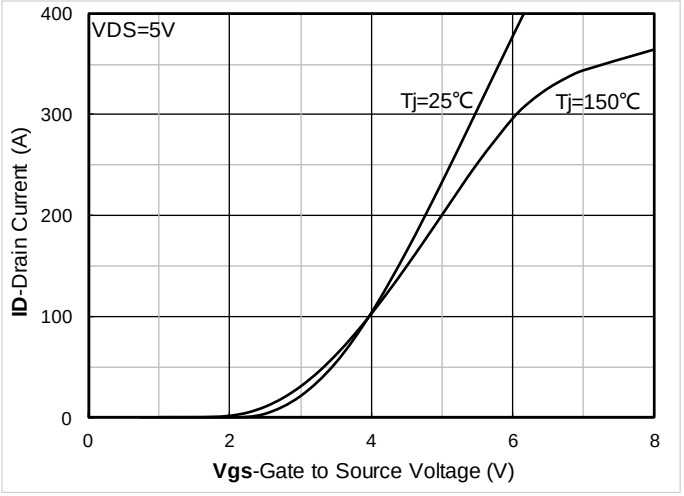


Figure 2. Transfer Characteristics

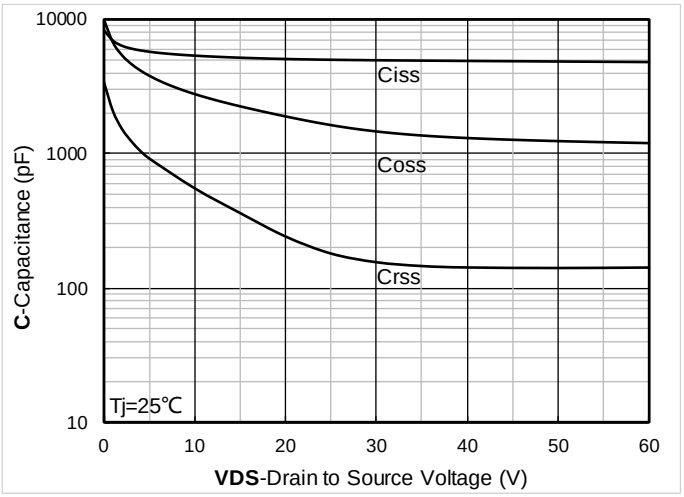


Figure 3. Capacitance Characteristics

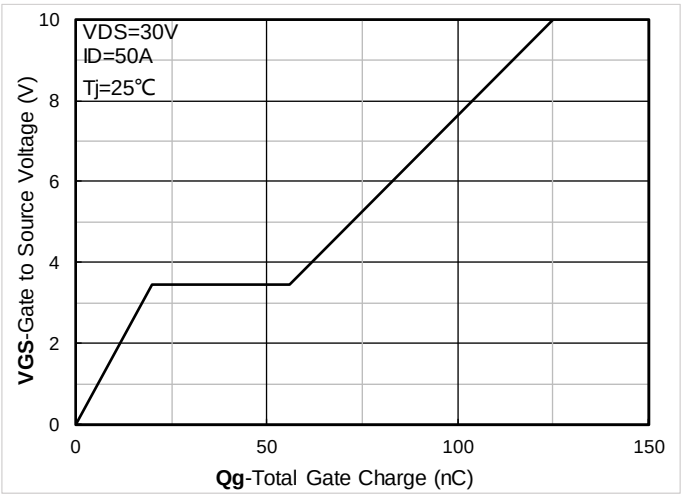


Figure 4. Gate Charge

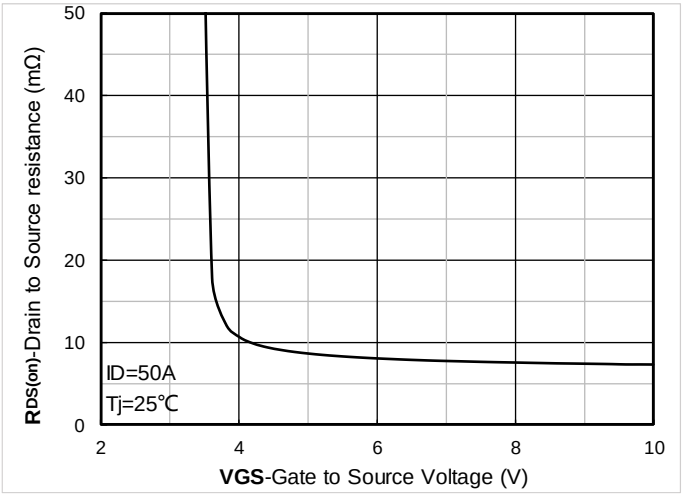


Figure 5. On-Resistance vs Gate to Source Voltage

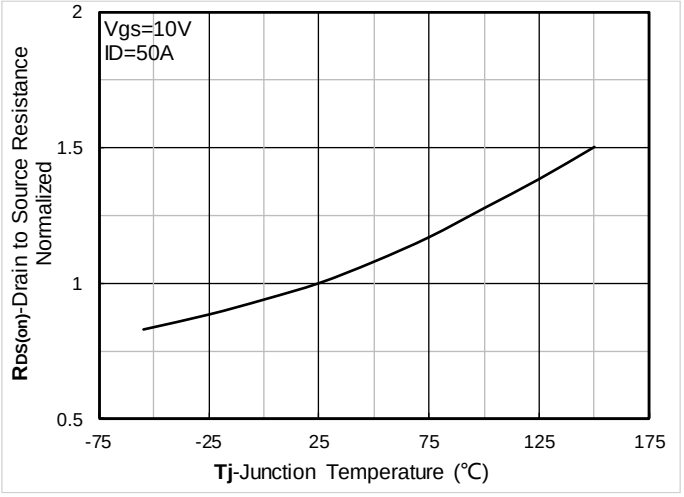


Figure 6. Normalized On-Resistance

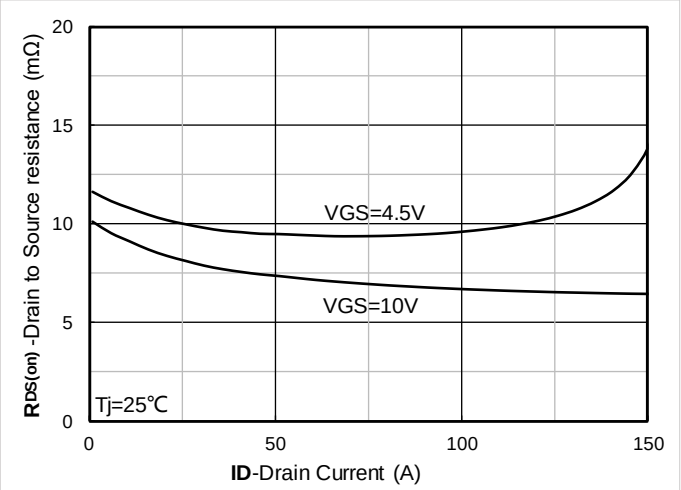


Figure 7. $R_{DS(on)}$ VS Drain Current

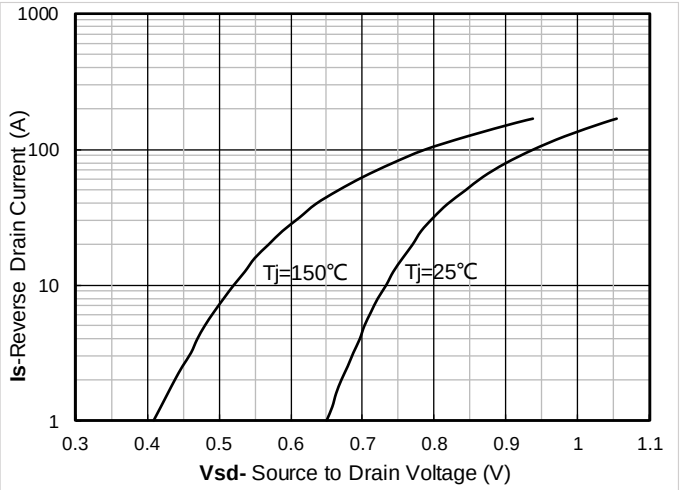


Figure 8. Forward characteristics of reverse diode

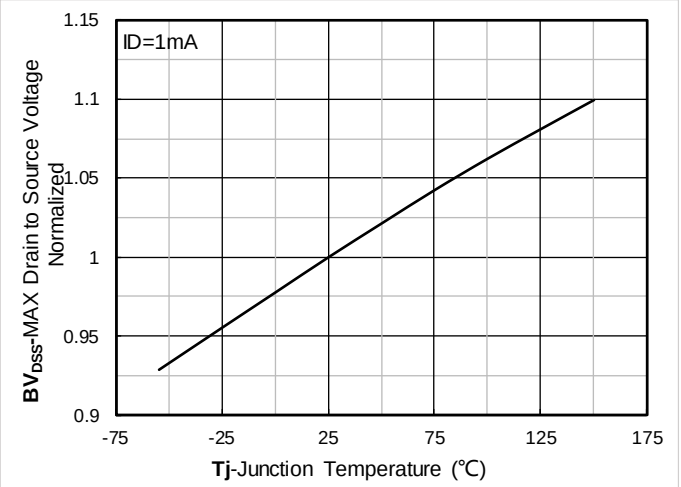


Figure 9. Normalized breakdown voltage

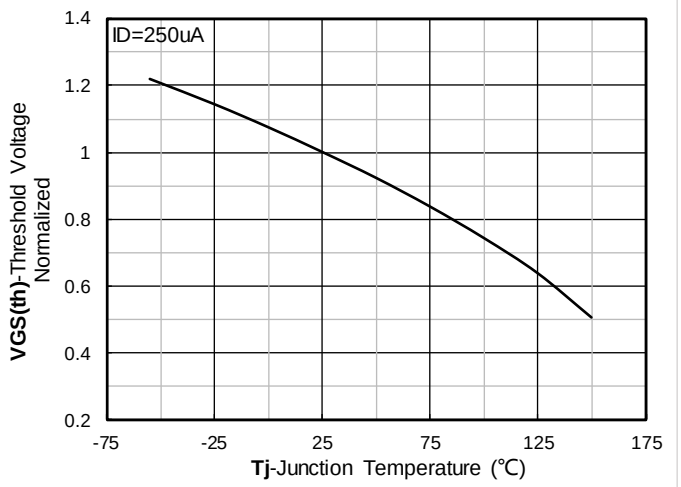


Figure 10. Normalized Threshold voltage

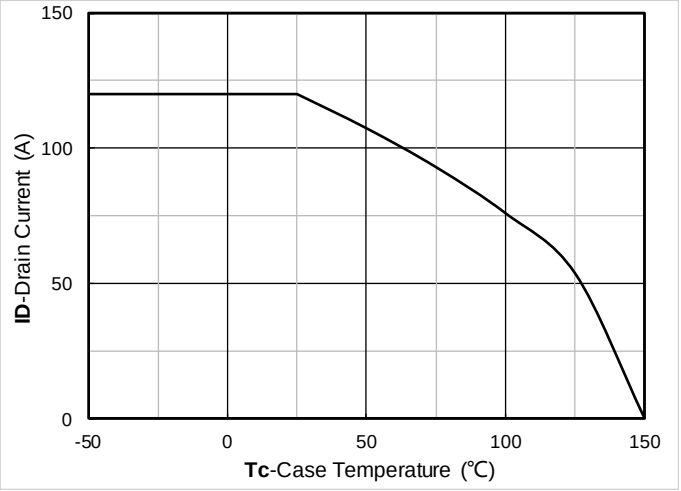


Figure 11. Current dissipation

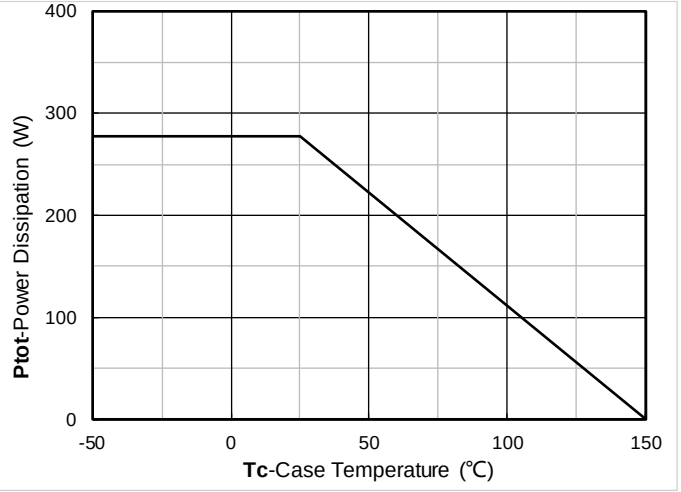


Figure 12. Power dissipation

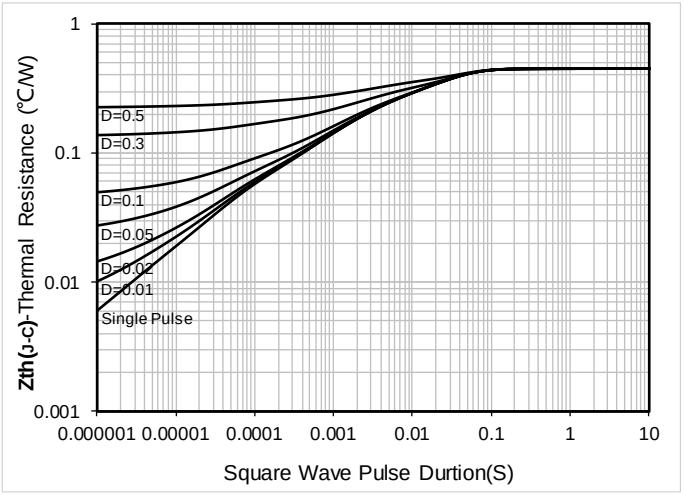


Figure 13. Maximum Transient Thermal Impedance

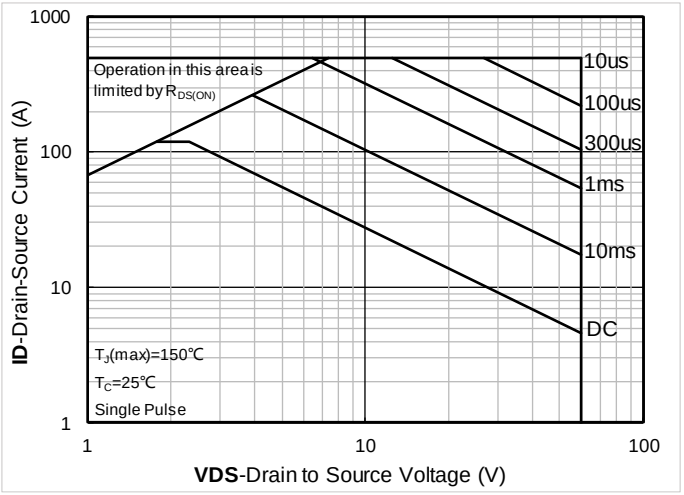


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

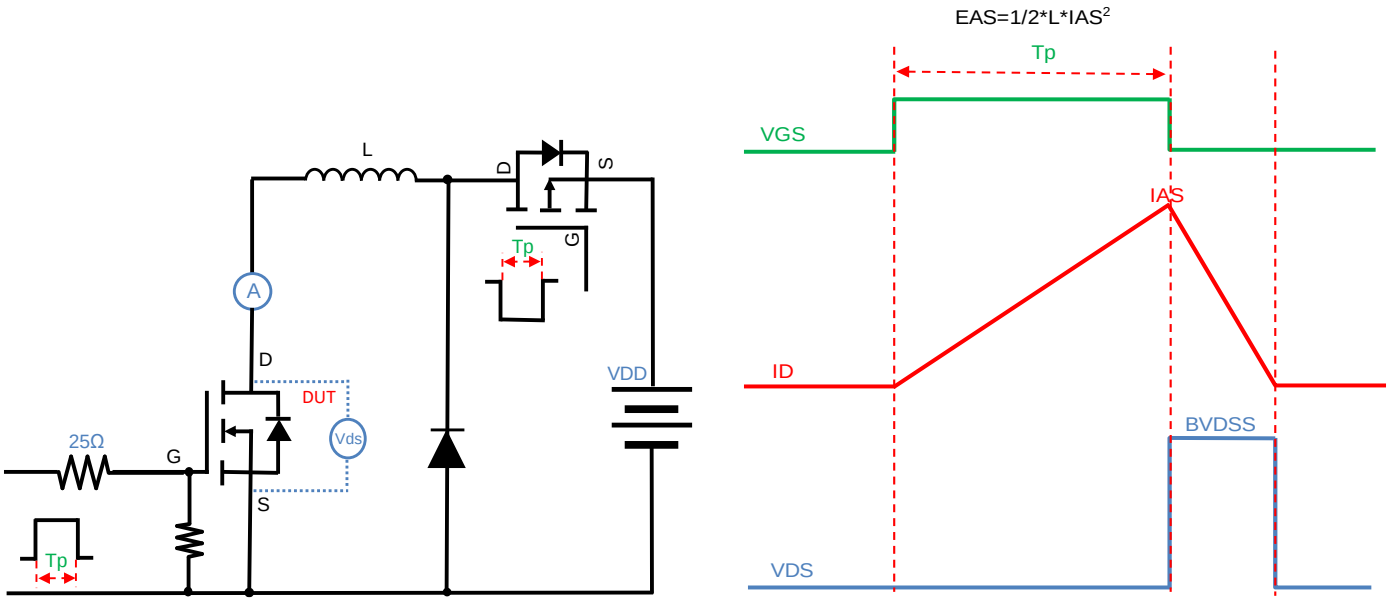


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

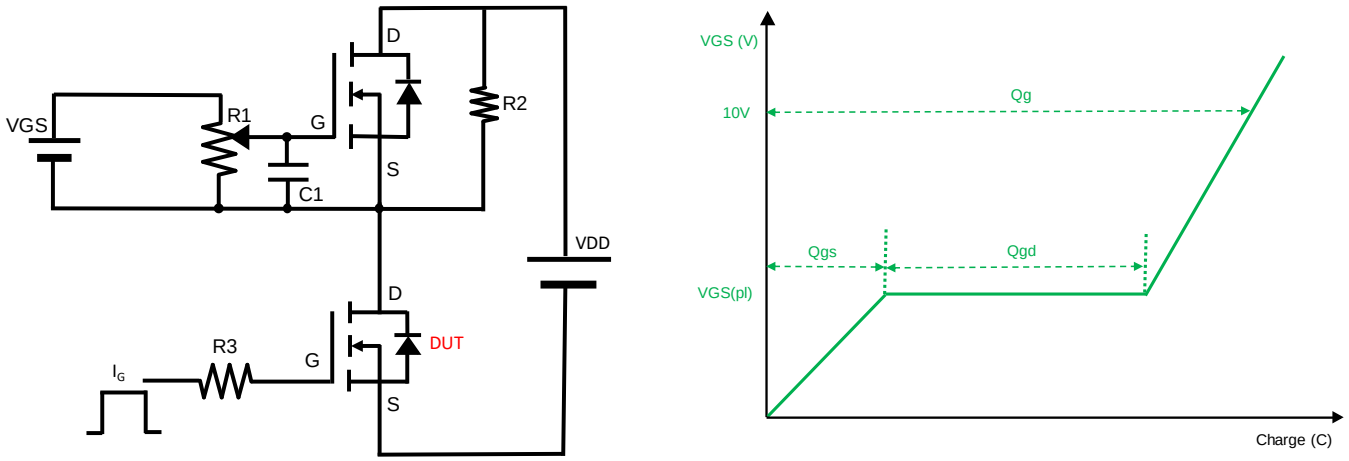


Figure B. Gate Charge Test Circuit & Waveform

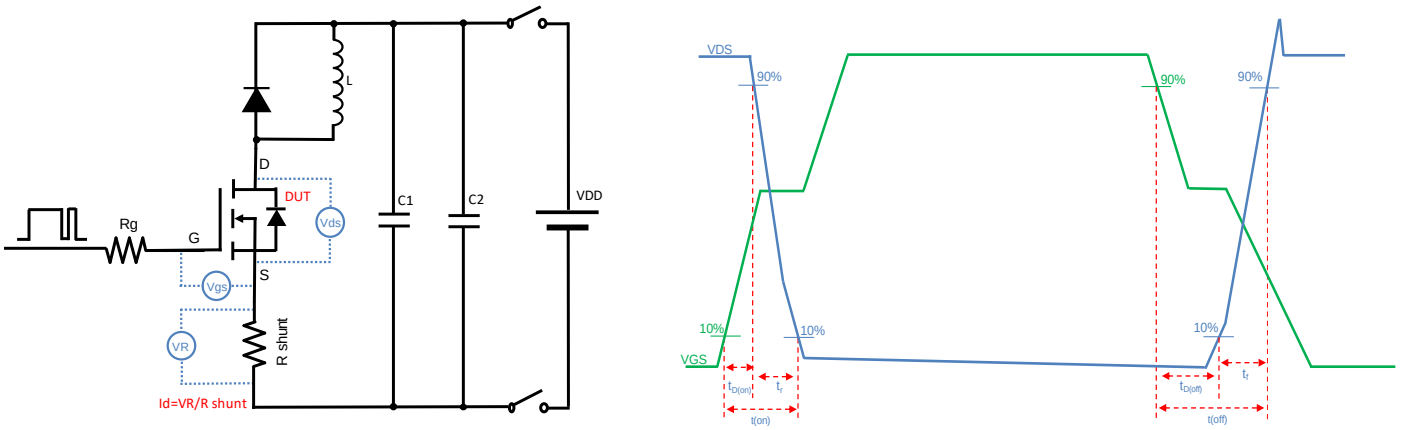


Figure C. Resistive Switching Test Circuit & Waveform

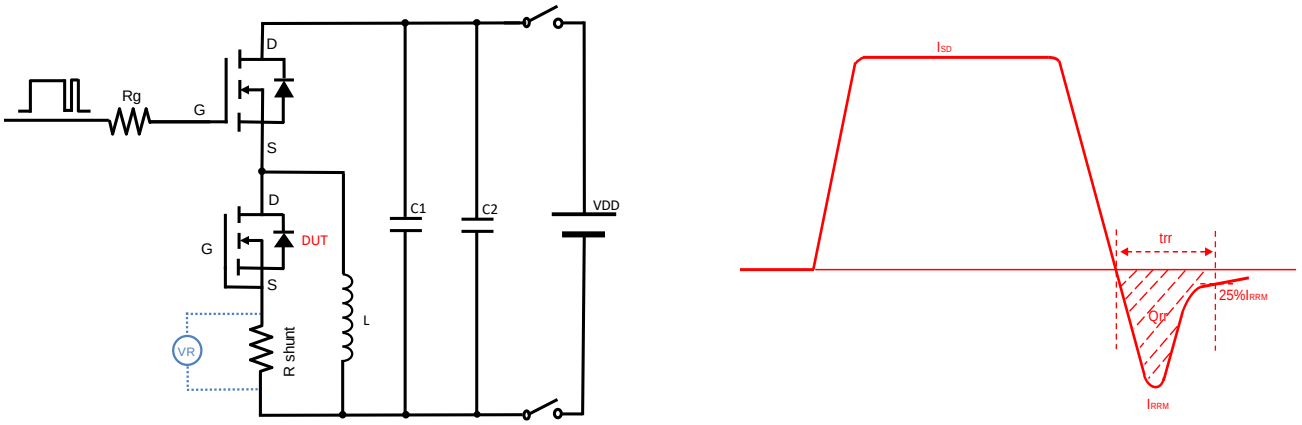
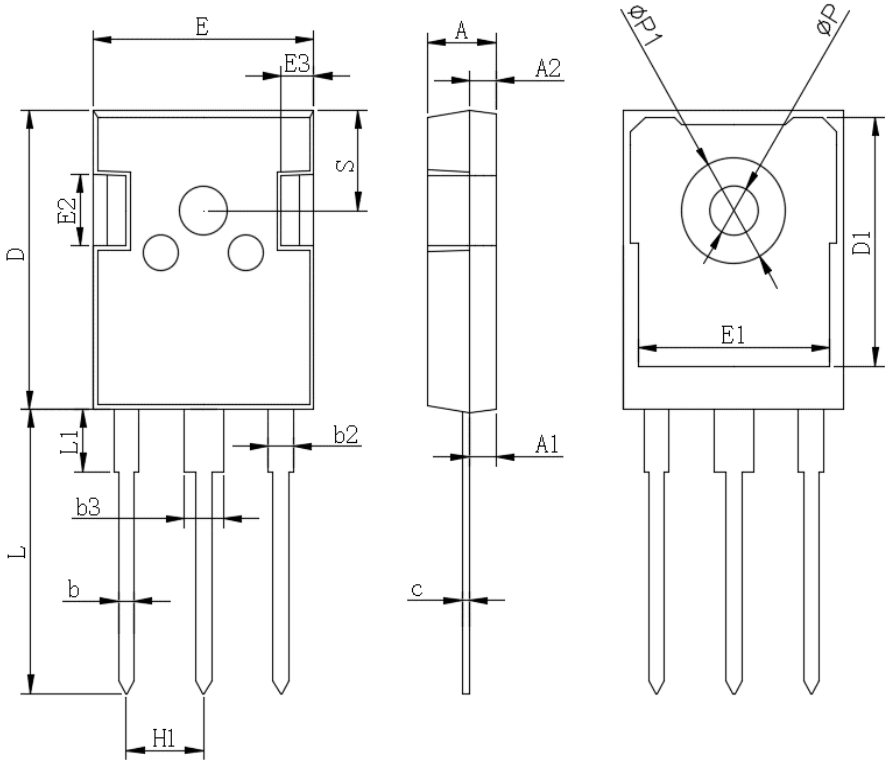


Figure D. Diode Recovery Test Circuit & Waveform

■ TO-247AB Package information

TO-247AB



TO-247AB		
Dim	Min	Max
A	4.80	5.20
A1	2.21	2.61
A2	1.85	2.15
b	1.0	1.4
b2	1.91	2.21
c	0.5	0.7
D	20.70	21.30
D1	16.25	16.85
E	15.50	16.10
E1	13.0	13.6
E2	4.80	5.20
E3	2.30	2.70
L	19.62	20.22
L1	-	4.30
ΦP	3.40	3.80
ΦP1	-	7.30
S	6.15TYP	
H1	5.44TYP	
b3	2.80	3.20

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1.0	2024.4.1	New release	Haijun Ding